What is Claimed is:

1. An input buffer circuit comprising:

first and second differential input terminals for receiving first and second input signals respectively, the difference between the input signals providing a differential input signal;

a first differential amplifier circuit having a first input coupled to the first differential input terminal and a second input coupled to the second differential input terminal, the first differential amplifier circuit being configured to generate a first logic level signal at an output node when the differential input signal is provided in accordance with a first digital I/O standard;

a second differential amplifier circuit having a first input coupled to the first differential input terminal and a second input coupled to the second differential input terminal, the second differential amplifier circuit being configured to generate a second logic level signal at the output node when the differential input is provided in accordance with a second digital I/O standard;

a first set of one or more switch circuits coupled to the first differential amplifier circuit, the first set of switch circuits selectively enabling the first differential amplifier circuit in a first input buffer mode; and

a second set of one or more switch circuits coupled to the second differential amplifier circuit, the second set of switch circuits selectively enabling the second differential amplifier circuit in a second input buffer mode.

2. The input buffer circuit of claim 1 wherein the first digital I/O standard has an input operating range and the first differential amplifier circuit is configured to generate the first logic level signal at the output node when the differential input is provided in accordance with the first digital I/O standard and a common mode component of the input signals is in a first portion of the input operating range, and wherein the input buffer circuit further comprises:

a third differential amplifier circuit having a first input coupled to the first differential input terminal and a second input coupled to the second differential input

terminal, the third differential amplifier circuit being configured to generate the first logic level signal at the output node when the differential input is provided in accordance with the first digital I/O standard and the common mode component of the input signals is in a second portion of the input operating range; and

a third set of one or more switch circuits coupled to the third differential amplifier circuit, the third set of switch circuits selectively enabling the third differential amplifier circuit in the first input buffer mode.

3. The input buffer circuit of claim 2 wherein the second digital I/O standard has an input operating range that extends above the input operating range of the first digital I/O standard.

4. The input buffer circuit of claim 3 wherein the first digital I/O standard is Low Voltage Differential Signaling.

5. The input buffer circuit of claim 4 wherein the second I/O standard is one of: current mode logic and pseudo current mode logic.

6. The input buffer circuit of claim 1 wherein each switch circuit receives a programmable control signal for selectively enabling the associated differential amplifier circuit.

7. The input buffer circuit of claim 1 wherein each of the first and second differential amplifier circuits comprises:

a first input transistor having a first terminal coupled to a biasing node, a second terminal, and a control terminal coupled to the first differential input terminal;

a second input transistor having a first terminal coupled to the biasing node, a second terminal, and a control terminal coupled to the second differential input terminal; and

a load circuit comprising

a first current mirror circuit having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to the output node, wherein the current at the first and second terminals of the first current mirror circuit are proportional to one another;

a second current mirror circuit having a first terminal coupled to the second terminal of the second input transistor and a second terminal coupled to a complementary output node, wherein the current at the first and second terminals of the second current mirror circuit are proportional to one another.

8. The input buffer circuit of claim 7 wherein the load circuit in each of the first and second differential amplifier circuits further comprises:

a third current mirror circuit having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to the second terminal of the second input transistor, wherein the current at the second terminal of the third current mirror is proportionally larger than the current at the first terminal of the third current mirror; and

a fourth current mirror circuit having a first terminal coupled to the second terminal of the second input transistor and a second terminal coupled to the second terminal of the first input transistor, wherein the current at the second terminal of the fourth current mirror is proportionally larger than the current at the first terminal of the fourth current mirror.

9. The input buffer circuit of claim 8 wherein, in each load circuit:

the first current mirror comprises

a first load transistor having a first terminal coupled to a supply signal node, a second terminal coupled to the second terminal of the first input transistor, and a control terminal coupled to the second terminal of the first input transistor, wherein the second terminal of the first load transistor provides the first terminal of the first current mirror, and

a second load transistor having a first terminal coupled to the supply signal node, a second terminal coupled to the output node, and a control terminal

coupled to the second terminal of the first input transistor, wherein the second terminal of the second load transistor provides the second terminal of the first current mirror;

the second current mirror comprises

a third load transistor having a first terminal coupled to the supply signal node, a second terminal coupled to the second terminal of the second input transistor, and a control terminal coupled to the second terminal of the second input transistor, wherein the second terminal of the third load transistor provides the first terminal of the second current mirror, and

a fourth load transistor having a first terminal coupled to the supply signal node, a second terminal coupled to the complementary output node, and a control terminal coupled to the second terminal of the second input transistor, wherein the second terminal of the fourth load transistor provides the second terminal of the second current mirror;

the third current mirror comprises

the first load transistor, wherein the second terminal of the first load transistor provides the first terminal of the third current mirror, and

a fifth load transistor having a first terminal coupled to the supply signal node, a second terminal coupled to the second terminal of the second input transistor, and a control terminal coupled to the second terminal of the first input transistor, wherein the second terminal of the fifth load transistor provides the second terminal of the third current mirror; and

the fourth current mirror comprises

the third load transistor, wherein the second terminal of the third load transistor provides the first terminal of the fourth current mirror, and

a sixth load transistor having a first terminal coupled to the supply signal node, a second terminal coupled to the second terminal of the first input transistor, and a control terminal coupled to the second terminal of the second input transistor, wherein the second terminal of the sixth load transistor provides the second terminal of the fourth current mirror.

10. The input buffer circuit of claim 9 wherein, in each of the first and second differential amplifier circuits, each input transistor is an NMOS transistor and each load transistor is a PMOS transistor, and wherein, for each input and each load transistor, the first terminal is a source terminal, the second terminal is a drain terminal, and the control terminal is a gate terminal.

11. The input buffer circuit of claim 7 further comprising:

a current source circuit having a first output that provides a first reference current to bias the biasing node of the first differential amplifier when the first differential amplifier is enabled and a second output that provides a second reference current to bias the biasing node of the second differential amplifier when the second differential amplifier is enabled.

12. The input buffer circuit of claim 11 wherein the current source circuit has a first input coupled to the first differential input terminal and a second input coupled to the second differential input terminal, and, when a common mode component of the differential input signal is above a threshold level, the current source circuit lowers the magnitude of the reference current provided to the enabled differential circuit as the common mode component of the differential input signal increases.

13. The input buffer circuit of claim 12 wherein the current source circuit comprises:

a first source input transistor having a first terminal coupled to a first current source node, a second terminal coupled to a second current source node, and a control terminal coupled to the first differential input terminal;

a second source input transistor having a first terminal coupled to the first current source node, a second terminal coupled to the second current source node, and a control terminal coupled to the second differential input terminal;

a first current source coupled between a supply signal node and the first output of the current source circuit, the first current source providing current into said first output only when the first differential amplifier circuit is enabled;

a second current source coupled between the supply signal node and the second output of the current source circuit, the second current source providing current into said second output only when the second differential amplifier circuit is enabled;

a first source current mirror circuit having a first terminal coupled to the first current source node and a second terminal coupled to the first output of the current source circuit, wherein the current at the first and second terminals of the first source current mirror circuit are proportional to one another; and

a second source current mirror circuit having a first terminal coupled to the first current source node and a second terminal coupled to the second output of the current source circuit, wherein the current at the first and second terminals of the second source current mirror circuit are proportional to one another.

14. The input buffer circuit of claim 11 further comprising:

a first bias current mirror circuit having a first terminal coupled to the first output of the current source circuit and a second terminal coupled to the biasing node of the first differential amplifier, wherein the currents at the first and second terminals of the first bias current mirror circuit are proportional to one another; and

a second bias current mirror circuit having a first terminal coupled to the second output of the current source circuit and a second terminal coupled to the biasing node of the second differential amplifier, wherein the currents at the first and second terminals of the second bias current mirror circuit are proportional to one another.

15. The input buffer circuit of claim 7 further comprising a pull-down current mirror circuit having a first terminal coupled to the complementary output node and a second terminal coupled to the output node, wherein the current at the first and second terminals of the pull-down current mirror circuit are proportional to one another.

16. An input buffer circuit comprising:

a first differential amplifier circuit receiving a differential input signal between a first input and a second input thereof, the first differential amplifier circuit being enabled

in a first input buffer mode to generate a first logic level signal at an output node when the differential input signal is provided in accordance with a first digital I/O standard; and

a second differential amplifier circuit receiving the differential input signal between a first input and a second input thereof, the second differential amplifier circuit being enabled in a second input buffer mode to generate a second logic level signal at the output node when the differential input signal is provided in accordance with a second digital I/O standard.

17. The input buffer of claim 16 further comprising:

a third differential amplifier circuit receiving the differential input signal between a first input and a second input thereof, the third differential amplifier circuit being enabled in the first input buffer mode to generate the first logic level signal at the output node when the differential input signal is provided in accordance with the first digital I/O standard;

wherein the first differential amplifier circuit provides greater amplification than the third differential amplifier circuit in a first portion of an input operating range for the first digital I/O standard, and the third differential amplifier circuit provides greater amplification than the first differential amplifier circuit in a second portion of the input operating range for the first digital I/O standard.

18. The input buffer of claim 17 further comprising:

a first set of one or more switch circuits coupled to the first differential amplifier circuit, the first set of switch circuits selectively enabling the first differential amplifier circuit in the first input buffer mode and disabling the first differential amplifier in the second input buffer mode;

a second set of one or more switch circuits coupled to the second differential amplifier circuit, the second set of switch circuits selectively enabling the second differential amplifier circuit in the second input buffer mode and disabling the second differential amplifier in the first input buffer mode; and

a third set of one or more switch circuits coupled to the third differential amplifier circuit, the third set of switch circuits selectively enabling the third differential amplifier

circuit in the first input buffer mode and disabling the first differential amplifier in the second input buffer mode.

19. The input buffer circuit of claim 18 wherein each switch circuit receives a programmable control signal for selectively enabling and disabling the associated differential amplifier circuit.

20. The input buffer of claim 17 wherein each of the first, second, and third differential amplifier circuits comprises:

a first input transistor having a first terminal coupled to a biasing node, a second terminal, and a control terminal providing the first input of said differential amplifier;

a second input transistor having a first terminal coupled to the biasing node, a second terminal, and a control terminal providing the second input of said differential amplifier; and

a load circuit comprising

a first current mirror circuit having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to the output node, wherein the currents at the first and second terminals of the first current mirror circuit are proportional to one another,

a second current mirror circuit having a first terminal coupled to the second terminal of the second input transistor and a second terminal, the current at the first and second terminals of the second current mirror circuit being proportional to one another, and

wherein in the first and second differential amplifier circuits the second terminal of the second current mirror is coupled to a first complementary output node, and in the third differential amplifier circuit the second terminal of the second current mirror is coupled to a second complementary output node.

21. The input buffer circuit of claim 20 wherein the load circuit in each of the first, second, and third differential amplifier circuits further comprises:

a third current mirror having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to the second terminal of the second input transistor, wherein the current at the second terminal of the third current mirror is proportionally larger than the current at the first terminal of the third current mirror; and

a fourth current mirror having a first terminal coupled to the second terminal of the second input transistor and a second terminal coupled to the second terminal of the first input transistor, wherein the current at the second terminal of the fourth current mirror is proportionally larger than the current at the first terminal of the fourth current mirror.

22. The input buffer circuit of claim 21 wherein:

in each of the first and second differential amplifier circuits, each input transistor is an NMOS transistor and the current mirror circuits comprise PMOS transistors; and

in the third differential amplifier circuit, each input transistor is a PMOS transistor and the current mirror circuits comprise NMOS transistors; and

for each input transistor, the first terminal is a source terminal, the second terminal is a drain terminal, and the control terminal is a gate terminal.

23. The input buffer circuit of claim 21 further comprising:

a pull-down current mirror circuit having a first terminal coupled to the first complementary output node and a second terminal coupled to the output node, wherein the current at the first and second terminals of the pull-down current mirror circuit are proportional to one another; and

a pull-up current mirror circuit having a first terminal coupled to the second complementary output node and a second terminal coupled to the output node, wherein the currents at the first and second terminals of the pull-up current mirror circuit are proportional to one another.

24. The input buffer circuit of claim 23 wherein the second digital I/O standard has an input operating range that extends above the input operating range of the first digital I/O standard.

25. The input buffer circuit of claim 24 wherein the first digital I/O standard is Low Voltage Differential Signaling and the second I/O standard is one of: current mode logic and pseudo current mode logic.

26. The input buffer circuit of claim 24 wherein each of the first and second input transistors in the first differential amplifier circuit has a lower conductivity than the first and second input transistors in the second differential amplifier circuit.

27. The input buffer circuit of claim 20 further comprising:

a first current source circuit having a first output that provides a first reference current to bias the biasing node of the first differential amplifier when the first differential amplifier is enabled and a second output that provides a second reference current to bias the biasing node of the second differential amplifier when the second differential amplifier is enabled; and

a second current source circuit having an output that provides a current to bias the biasing node of the third differential amplifier when the third differential amplifier is enabled.

28. The input buffer circuit of claim 26 wherein the first current source circuit receives a differential input signal between a first input and a second input thereof and, when a common mode component of the differential input signal is above a threshold level, the first current source circuit lowers the magnitude of the reference current provided to the enabled differential circuit as the common mode component of the differential input signal increases.

29. A method of receiving a signal transmitted according to one of a plurality of differential I/O standards, comprising:

setting one or more control signals in an input buffer circuit to specify one of a plurality of input buffer circuit modes, each mode corresponding to a predetermined differential I/O standard;

enabling at least one differential amplifier circuit in the input buffer circuit in response to the setting of the one or more control signals, each of the at least one enabled differential amplifier circuits being compatible to receive input signals provided in accordance with the differential I/O standard of the specified input buffer circuit mode; and

disabling at least one other differential amplifier circuit in the input buffer circuit in response to the setting of the one or more control signals.

30. The method of claim 29 wherein each of the differential I/O standards corresponding to the plurality of input buffer circuit modes has a different input operating range.

31. The method of claim 29 comprising programmably setting the one or more control signals.